

# Low-power design solutions

**Holly Stump** analyses the decisive importance of low-power design and power emerging as a key competitive advantage in portable and consumer markets

**T**hose attending the sessions and walking the aisles of the VLSI show in Bangalore this year saw an overwhelming focus on the critical importance of low-power design.

We see power emerging as a key competitive advantage in portable and consumer markets, driven by the increasing importance of battery life in a wide spectrum of products. For high-volume consumer/computer/multimedia applications, costs of IC packaging, system packaging and cooling track strongly with power dissipation. At 90 nm and below, power becomes even more critical. Without proper power management and power-grid design, there can be catastrophic functional failures, timing problems and signal-integrity issues. This dictates a complete power signoff, otherwise NREs go up; market windows are missed; market share decreases and start-ups sink or giants stumble.

Santa Clara – Total power, leakage power, EM (electro migration) and dynamic voltage

drop are the biggest concerns for SoC designers today, according to the majority of respondents to a survey conducted by low-power design solutions leader Sequence Design. A very even distribution of 25 per cent of the responses noted each of these four parameters as critical in design closure and signoff.

Many analysts have tracked process node migration statistics; this sample showed the highest growth rate at the 65 nm process node even though the majority of designs are still thriving at 90 nm.

Low power seems to be on everybody's mind these days: the most frequently stated concern was achieving the power specs for their SoC (38 per cent) followed by battery life (26 per cent), IC packaging costs (15 per cent), reliability (12 per cent) and yield (nine per cent.)

To minimise power overall, it is critical to address power management early in the design cycle, at RTL or above. Today's designers meet the challenge with a variety of techniques to be challenged with several criteria to manage power. One is architectural what-if analysis, where multiple architectures are explored for best power/performance/area. This can best be done at ESL or at RTL. Next, the most popular techniques to manage power are:

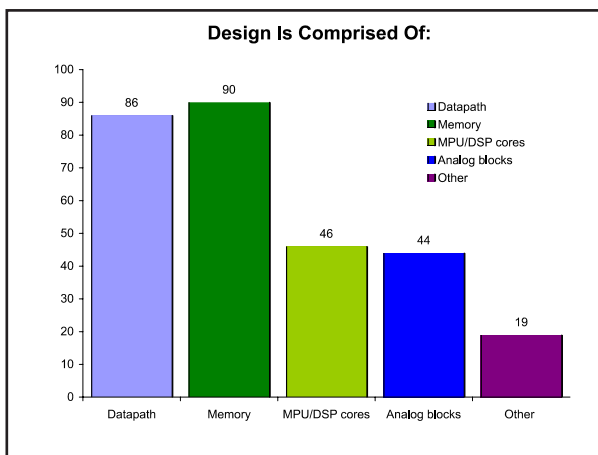
clock gating (24 per cent); multi-Vt libraries (22 per cent); power gating (15 per cent); voltage islands (13 per cent) and clock power optimisation (13 per cent) – (respondents were allowed to specify more than one technique).

## Examples of silicon-aware power optimisation

One power-optimisation technique utilises a power-estimation tool to measure the effects of clock gating. The designer simply defines the conditions under which clock gating should be applied and the tool applies the appropriate clock-gating cells, specifying which registers are gated, as well as the power-consumption effects.

Another technique is the use of mixed threshold-voltage (VT) cells.

Higher-performance circuits often use low-VT cells at the expense of higher leakage, but an easy-to-implement optimisation technique is the use of multi-threshold voltage cells. An early RTL power-estimation methodology can predict leakage based on the mix of low-VT and high-VT cell population expectations. Yet another power-management technique involves using voltage islands, which supply different voltages to different parts of the design—for instance, the functional core and the input/output (I/O) ring. Since power is proportional to  $V^2$ , even a modest reduction in supply voltage to blocks with non-critical timing can significantly reduce power consumption.




# Power

Specifically, reducing the supply voltage from VHIGH to VLOW results in a power consumption of Thus, changing the supply from 1.2 V to 0.9 V reduces power consumption by approximately 44 per cent. Again, an RTL power-estimation tool can measure the effects of multiple voltage island configurations.

Another effective optimisation is the use of power gating, which puts various functional domains in the design into 'sleep' mode when not required. With an appropriate power-estimation tool, the user can perform multiple 'what-if' analyses to determine the optimum power-gating scheme. Gautami Bhattacharjee, channel marketing at Sequence Design, commented, "More than 50 per cent of the respondents manage power through both front end design and back end implementation efforts, resulting in equal product interest in for Sequence Design's PowerTheater™ and Cool Products™."

Regarding design elements, besides data path and memory, around half of the most of the designers canvassed used a high percentage of data path, commercial or internally developed MPU / DSP cores and 44 per cent designed/used analogue blocks. For most, the language of design still means Verilog, the language of choice for almost 50 per cent System Verilog with 20 per cent, or VHDL with nine per cent. For higher-level design, 16 per cent reported designing in System C or C++. In conclusion, general comments from designers favoured power management tools across the board, especially for RTL power analysis; accuracy; power estimation for emerging power techniques, visual power debug; wasted power detection; integrated tool flows; vectorless

power estimation; power analysis tools that support power gating; and basically everyone would like to achieve faster results! The survey results are based on 115 responses. The industry sectors most represented among survey respondents are wireless telecommunications (31 per cent), portable electronics equipment (21 per cent) and computer networking (27 per cent.) At Sequence, we recognised early on that power would be a significant barrier to design success. For example, PowerTheater remains the only RTL analysis and management solution, and was preferred for power management by nearly 70 per cent of respondents. Customers from around the world in various application segments have been telling us about the challenges they are facing in terms of managing power issues as early in the design phase as possible. At the VLSI show, our Silicon Aware PowerTheater 65 was demonstrated, with tremendous new features for multi-voltage islands, mixed voltage threshold, power gating, and clock gating. PowerTheater 65's capabilities include accurate RTL power analysis closely correlated to actual silicon; power management tools that allow designers to reduce power at RTL using 'what-if' scenarios and make early tradeoffs at the architectural level; power vector forward technology to select vectors for downstream analysis, feeding them to later stages of the design cycle for gate-level verification and voltage-drop analysis and gate-level power verification, preventing power creep. Some PowerTheater customer applications include the mixed signal Wi-Fi device-a multi-million-gate design-which was developed

by Airgo, a wireless connectivity company that invented the multiple-input, multiple-output (MIMO) technology for next-generation Wi-Fi. The design achieves IEEE 802.11 a/b/g compliance, integrating a 2x3 MIMO system, PHY and MAC layers, as well as analog-to-digital converters and digital-to-analog converters-all on one chip. Cradle Technologies, a fabless semiconductor company that develops multi-core DSP (MDSP) for next-generation multimedia applications, designed the MDSP. The chip deploys 16 DSPs and eight general-purpose processors to encode 16 channels of MPEG4 SP@L3 and more. Sequence also showcased its Cool products, consisting of Cool Time, Cool Power, and Cool Check. Cool Time/Cool Power are concurrent and SI-aware, enabling fast design closure times by preventing time-consuming iterations between separate timing, SI and power analysis and optimisation tools. These products also help manage power through a variety of reduction techniques. Also on display was Cool Check, the first and only formal power grid verification tool, enabling designers to check 100 per cent of all power grid connections, rapidly detecting errors that both static and dynamic voltage-drop solutions fail to find. Sequence continues to define 'leadership' in low-power design. This is evidenced by customer satisfaction at more than 150 sites worldwide, a long-time commitment to serious science resulting in true breakthrough products and beneficial relationships with foundries and other EDA companies to insure interoperability and ease of use. 

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